CLAIMS

What is claimed is:

1. A multiple processor integrated circuit comprises:

a first processor coupled to a first cache;

a first interface coupled to receive memory references that miss in the first cache;

a second processor coupled to a second cache;

a second interface coupled to receive memory references that miss in the second cache;

common circuitry coupled to the first interface and to the second interface;

a first power terminal coupled to provide power to the first processor; and

a second power terminal coupled to provide power to the second processor.

2. The multiple processor integrated circuit of Claim 1, wherein the first interface is configured to permit operation of the second processor when the first power terminal is not powered.

3. The multiple processor integrated circuit of Claim 2, wherein the second interface is configured to permit operation of the first processor when the second power terminal is not powered.

4. The multiple processor integrated circuit of Claim 3, further comprising:

a third power terminal coupled to provide power to the common circuitry; and

wherein the common circuitry comprises a memory bus interface.

5. The multiple processor integrated circuit of Claim 4, further comprising a third processor coupled to a third cache, and a fourth processor, coupled to a fourth cache; wherein the third processor and third cache are coupled to a fourth power terminal, and the fourth processor and fourth cache are coupled to a fifth power terminal, and wherein

6. The multiple processor integrated circuit of Claim 4, wherein the first interface is designed such that no signals driven by gates powered by the third power terminal are connected to any P-diffusion located in an N-well that is electrically connected to the first power terminal;

7. A system comprising:

a multiple processor integrated circuit further comprising:

a first processor coupled to a first cache,

a first interface coupled to receive memory references that miss in the first cache,

a second processor coupled to a second cache,

a second interface coupled to receive memory references that miss in the second cache,

common circuitry coupled to the first interface and to the second interface,

a first power terminal coupled to provide power to the first processor, and

a second power terminal coupled to provide power to the second processor;

a first power supply coupled to the first power terminal of the multiple processor integrated circuit;

a second power supply coupled to the second power terminal of the multiple processor integrated circuit; and

a system controller coupled to the common circuitry of the multiple processor integrated circuit, to a system memory, and I/O circuitry

8. The system of Claim 7, wherein the first interface of the multiple processor integrated circuit is configured to permit operation of the second processor when the first power terminal is not powered.

9. The system of Claim 8, wherein the first power supply is coupled to the I/O circuitry, and wherein the first power supply can be turned off under command of the I/O circuitry.

10. The system of Claim 9, wherein the second power supply is coupled to the I/O circuitry, and wherein the second power supply is capable of being set to a first and a second operating voltage.